Voltage Tuned Dielectric Resonance 20.5GHz Harmonic Oscillator with Novel Structure

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ABSTRACT

This paper presents a voltage controlled K-band harmonic oscillator composed of two X-band dielectric resonator circuits at the input port and the output port of the oscillator The novel structure supplies not only a voltage tuning circuit but also an output port at fundamental frequency as a function of prescaler on the structure. The output frequency is 20.5GHz and the maximum power level of the output is +5.5dBm. The harmonic oscillator exhibits -30dBc of fundamental frequency rejection.

INTRODUCTION

For the digital communications and broadcasting via satellites, their ground station uses usually dielectric resonance oscillators(DRO) or phase locked dielectric resonance oscillators(PLDRO) as the stable microwave frequency source. The K/Ka-band (18~40GHz) multipurpose satellites also need microwave frequency sources with high stability and low phase noise for their high quality transceiver system on the ground system. Their recommended type is the push-push type [1],[2],[3] and this type is to overcome the limitation on device capabilities and fabrication techniques at higher microwave frequencies. For the push-push structure, two identical oscillators should be arranged in the push-push configuration of an oscillator that is twice the frequency of each individual oscillator.

However, the configuration of the push-push type oscillator is complex and not easy to control the ideal balance of each composed oscillator to reject a fundamental frequency component sufficiently. These are sometimes serious for commercial fabrication. With these reasons, a harmonic oscillator can be used instead of such type, but ordinary harmonic oscillators have components of strong power of fundamental frequency and lower power of harmonic frequency. These problems are more serious than those of the push-push type. The purpose of a work on this paper is to introduce the study of analysis to maximize harmonic frequency generation and fundamental frequency suppression and the design of a voltage controlled dielectric resonance 20.5GHz harmonic oscillator with novel structure. This has better performance and benefits than those of push-push type in real application. This oscillator applied on phase locked loop(PLL) is shown in Fig. 1.

TH 3B

THEORY

Nonlinear elements of an device sometimes make unwanted signal distortion but ordinary harmonic oscillators basically want this distortion. However, this is not so enough. To solve this problem, a bias condition is considered to maximize the harmonic oscillation. When the nonlinear equivalent circuit of GaAs MESFET with peripheral circuits is shown in Fig. 2, the oscillator can be biased at a point of V_{GS}=0 where the generated fundamental frequency signal is halfwave voltage rectified by the forward conduction of gate at the device. From Gopinath's nonlinear equation, the current I_{ds} is shown in Fig. 3 with frequency components in time domain, where it shows that this makes harmonic generation with

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class A current rectification at drain. Similarly, the class B bias of $V_{GS}=V_p$ can also make harmonic generation with high efficiency. However, it is considered that this can not supply higher oscillated signal power than the class A bias.

The matching circuit, which is a load, should be selected and designed to maximize the wanted harmonic component. In reality, the generation of the 2nd harmonic signal at class A bias is dependent on both of a load, R_l, and an output conductance, G_{ds}, at drain. Their effect is explained with the control of R_l and G_{ds}. Under class A bias, the effects of equivalent components like R_d, L_d, C_{dg}, R_s, L_s are disregarded as small. As the cases for simulation, G_{ds}=0.12 mho at V_{ds}=+3V and V_{gs}=-1.3V, and G_{ds}=0.16 mho at V_{ds}=+3V and V_{gs}=-0.2V are selected[4]. The result of simulation shows that the nonlinear behavior of V_{ds} is increased as the values of G_{ds} and R_l are increased. This is shown in Fig. 4. As G_{ds} already has the maximum value on class A bias, the harmonic generation can be maximized with the control of R_l. If the load is nearly an open circuit at fundamental frequency, the oscillator can generate maximum harmonic power. For satisfying this load, a dielectric resonator (DR) is proposed.

DESIGN

The 20.5GHz harmonic oscillator is designed on the base of 10.25GHz DRO circuit configuration. The schematic diagram is shown in Fig. 5. As an active device, a packaged HEMT, FHX35LG, is used. A cylinder type $TE_{01\delta}$ mode DR is used for resonators. DC bias point is selected at V_{GS}=-0.2V and V_{DS}=+3V, I_{DS}=30mA[5]. For supplying a bias without disturbing the harmonic generation, it uses a RF choke working at the fundamental frequency as well as the 2nd harmonic frequency.

This first DR, which is double microstrip coupled, controls the frequency of oscillation with using a silicon varactor diode having the junction capacitance of 2.5pF at zero bias condition. The second 10.25GHz dielectric resonator is a matching circuit. This circuit has DC bias blocking discontinuity which has the role of bandpass filtering at 20.5GHz. This second DR is double microstrip coupled. This structure gives the output port of the fundamental frequency signal at the harmonic oscillator as the role of ½ frequency divider or ½ prescaler. With this structure, the PLL circuit doesn't need an extra K-band frequency divider anymore.

The resonance frequency and the coupling factor, β, of DR are calculated with the algorithm modified from the results of Mogina, Posieszalski and Chaubet[6]. The harmonic oscillator is fabricated on a teflon substrate, whose relative dielectric constant is ε_s=2.5, dielectric height is h=0.508mm, and thickness of copper is t=0.08mm. DR whose parameters are ε_r=3.8, radius a=2.75mm, height h_2=2.44mm, and unloaded quality factor Q_r=105/(2f_o+2.6), is used in this design.

The linearly designed oscillator is evaluated with the nonlinear analysis of harmonic balance method. The fabricated harmonic oscillator is shown in Fig. 6. The harmonic oscillator is fabricated on a teflon substrate with the size of 33x40mm^2. PCB is placed in the cavity of 43.4x36.4x21mm^3 with two metal tuning plate for frequency control.

MEASURED RESULTS

The measured spectral performance of the oscillator is shown in Fig. 7. The output frequency is able to be around 20.5GHz with mechanical tuning and the maximum power level of output is +5.5dBm. It should be noted that the fundamental and the 3rd harmonic frequency component are suppressed with enough and these are typically less than -30dBc and -24dBc, respectively. The voltage tuned frequency range of the oscillator is 54MHz at 0~3.5V tuning voltages. This is fully enough for PLL application at a fixed frequency signal source because the frequency drift of ordinary commercial DROs at Ku-band is usually under $\pm$1.5MHz on their specification. The FM(SSB) phase noise is below -90dBc/Hz, which is measured at the offset frequency of 100kHz under free running condition. This result satisfies phase noise requirement of IESS (INTELSAT Earth Station Standard) for digital satellite communications with data rates below 2.048Mbps. The output performance as the function of tuning voltages is shown in Table 1.

These results show better performance than +3dBm maximum at output power and -14dBc at fundamental frequency rejection of the push-push type voltage tuned DRO reported by Liu and Ho.

CONCLUSION

A harmonic oscillator at K-band for digital satellite communications was fabricated for a commercial product. The structure has a voltage controlled circuit for PLL application and an output port of ½ prescaler for fundamental frequency output. The proposed oscillator has a simple structure and several functions for PLL application, and it is easy to control the fabrication. This oscillator is utilized in the PLL frequency sources of the transmit block upconversion or low noise block downconversion for K/Ka-band digital communications and satellite broadcasting.

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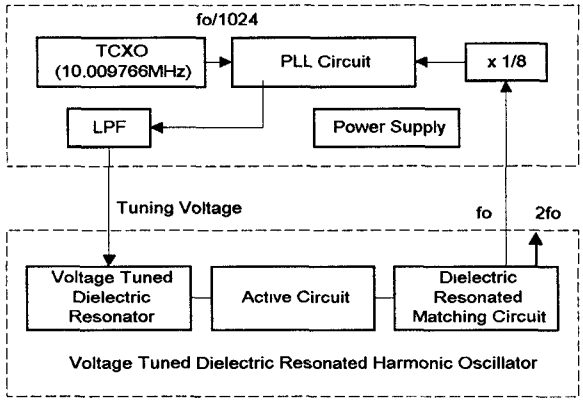


Fig. 1. Structure of proposed resonance harmonic oscillator and PLL circuit.

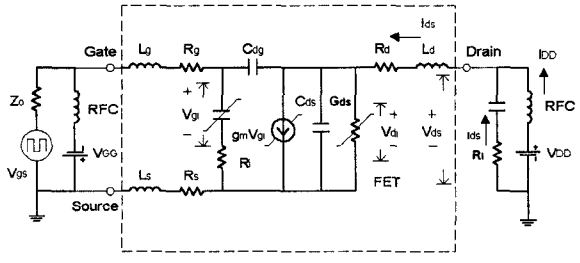


Fig. 2. Nonlinear equivalent circuit of GaAs MESFET of proposed harmonic oscillator.

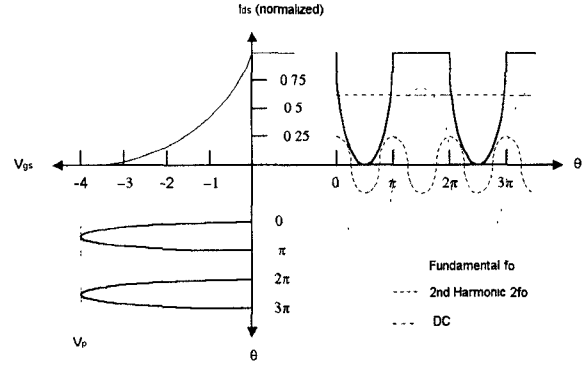
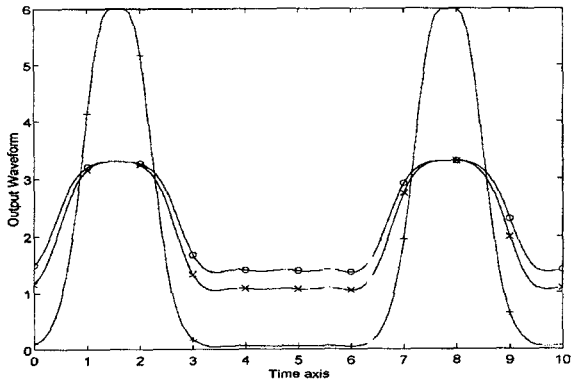


Fig. 3. Harmonic generation due to class A biased waveform rectification from fundamental signal.



Rl=10, *Gds*=0.12 : -o-, *Rl*=10, *Gds*=0.16 : -x-, *Rl*=100, *Gds*=0.16 : -+-

Fig. 4. Output voltage, V_{ds}, dependent on load, R_l, and output conductance, G_{ds}, of drain.

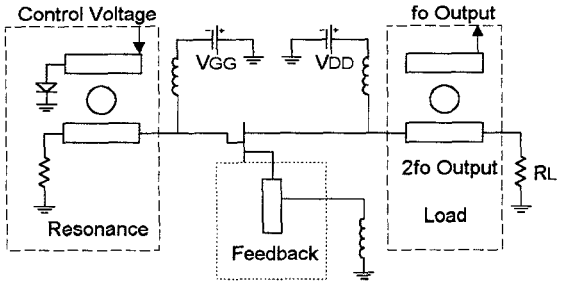


Fig. 5. Schematic diagram of proposed harmonic oscillator with dual resonance.

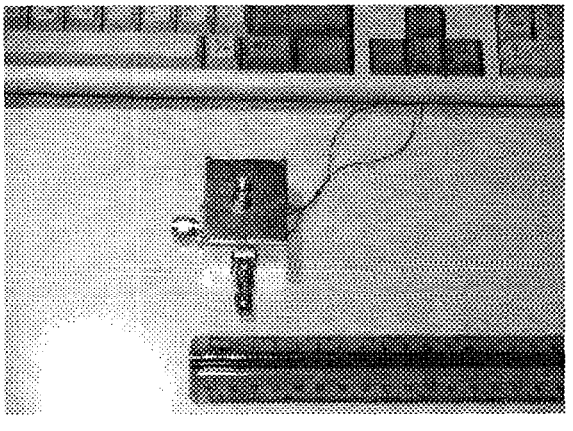


Fig. 6. Ficture of 20.5GHz harmonic oscillator.

Table 1. Voltage controlled response of oscillator.

Control Voltage (V)	Osc. Freq. (GHz)	Harmonic Power (dBm)	Fundamental Suppression (dBc)	PLL Output port (dBm)
0	20.6163	+1.33	-11.50	-10.33
1	20.6067	+1.50	-16.33	-5.67
1.5	20.5847	+2.17	-23.33	-4.50
2	20.5723	+2.67	-25.66	-3.83
3	20.5637	+3.00	-29.00	-3.17
3.5	20.5623	+3.33	-30.17	-3.00

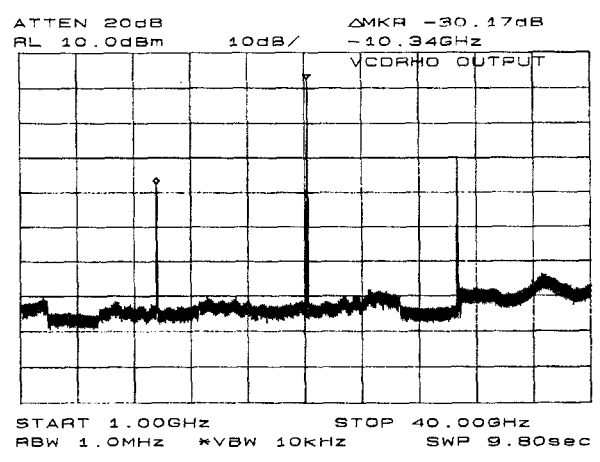


Fig. 7. Measured output spectral performance of proposed oscillator.